Feature

Switched-Capacitor Circuits

Gabor C. Temes, Un-Ku Moon, and David Allstot

©SHUTTERSTOCK.COM/PIXELS HUNTER

The first publication of a switched-capacitor resistor occurred nearly 150 years ago in James Clark Maxwell's pioneering book *A Treatise on Electricity and Magnetism* [1]. He pointed out that the average current through a periodically inverted capacitor C remains the same when it is replaced by a resistor of value $R = T/2C$, where T is the period of inversions. He used this equivalence to give a method for measuring capacitance using a circuit employing a battery and galvanometer. The next publication came nearly a century later, when D. L. Fried proposed the idea of sampled-data analog filters [2], containing only switches, capacitors and (if necessary) amplifiers. His paper showed how to realize the equivalent of a resistor using two switches and a capacitor. A motivation for using such circuits may be found from the history of analog filters. These were developed for telephony, and used initially resistors, capacitors and inductors. Inductors were bulky and lossy, and were replaced at the earliest opportunity by alternative circuits using amplifiers. The resulting active-RC filters were realized by discrete elements: capacitors, resistors and integrated-circuit amplifiers. With the development of integrated-circuit technology, there was strong motivation to put these filters on a single-substrate IC. However, the *absolute* values of resistors and capacitors could only poorly be controlled by the fabrication process: errors of 20-30% were common. Since the errors of resistors and capacitors were not tracking each other, the errors of time constants given by RC products were unacceptably high. This made their frequency responses unpredictable. Trimming could be used to tune such filters, but this was expensive. When the resistors were replaced by their switched-capacitor (SC) equivalents, the RC time constants were replaced by time constants of the form TC_1/C_2. Since the switching period T can be accurately controlled, as can the ratio of on-chip capacitors, the SC filters (SCFs) could be implemented with high accuracy. The design of such filters initially was based on those of active-RC ones, but it was soon recognized that they can be more effectively designed directly in the sampled-data domain, in terms of the z variable, similarly to digital filters. Although other design techniques exist, the most popular one constructs

Digital Object Identifier 10.1109/MCAS.2021.3118195
Date of current version: 12 November 2021

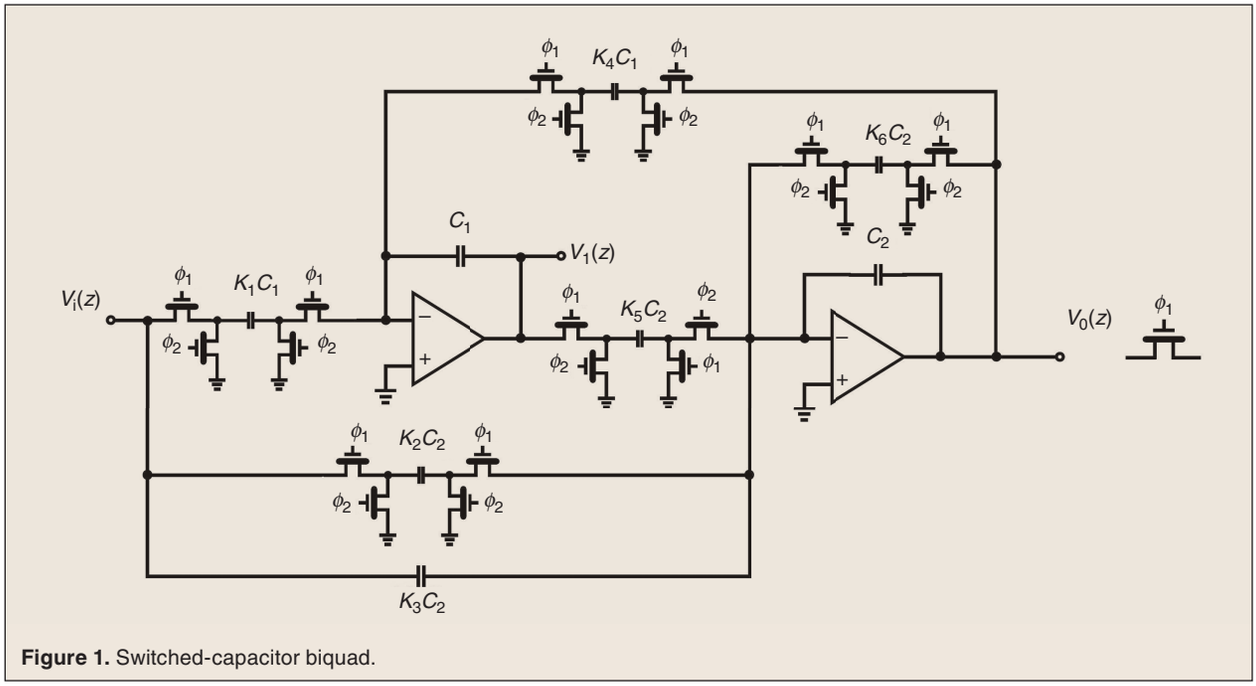

Figure 1. Switched-capacitor biquad.

higher-order filters as a cascade of lower-order sections, such as biquadratic filter or "biquad" shown in Figure 1.

Although filters were the first SC circuits implemented, it was soon recognized that other analog circuits are also accessible for switched-capacitor realization [3]. These included gain stages, modulators, PLLs, ADCs and DACs, oscillators and VCOs, and many others. Essentially, all analog IC stages at low or medium frequencies can be implemented using SC circuitry. In some cases, however, continuous-time (CT) realization lead to better performance. This may be due to the high bandwidth requirements on the amplifiers due to the impulsive charge redistribution operation, and the nonideal effects associated with all components. Some of these effects are listed below, with existing methods that can mitigate them.

Switches are subject to charge injection. This is due to the exit of the charges stored in the channel during conduction. The channel charge Q_{ch} may be estimated from the formula $Q_{ch} \times R_{on} = L^2/\mu$, where R_{on} is the on-resistance of the switch, L is the length of the channel, and μ the carrier mobility in it [4]. Charge injection may be mitigated by using transmission gates rather than single switches or by adding dummy devices ([5], p. 448). For a floating switch operating at a signal voltage, both Q_{ch} and R_{on} will be signal dependent, and hence introduce nonlinear distortion. There are several situations requiring different mitigation strategies, discussed

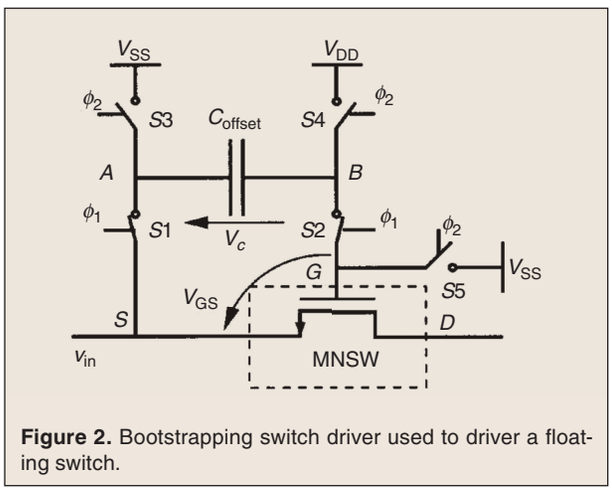

Figure 2. Bootstrapping switch driver used to driver a floating switch.

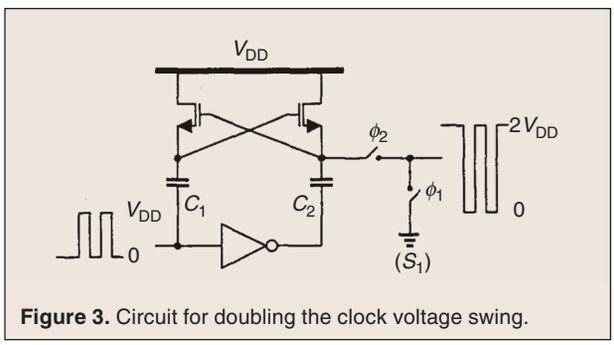

Figure 3. Circuit for doubling the clock voltage swing.

Gabor Temes, Un-Ku Moon and David Allstot are professors at the School of Electrical Engineering and Computer Science, Oregon State University, Corvallis, Oregon.

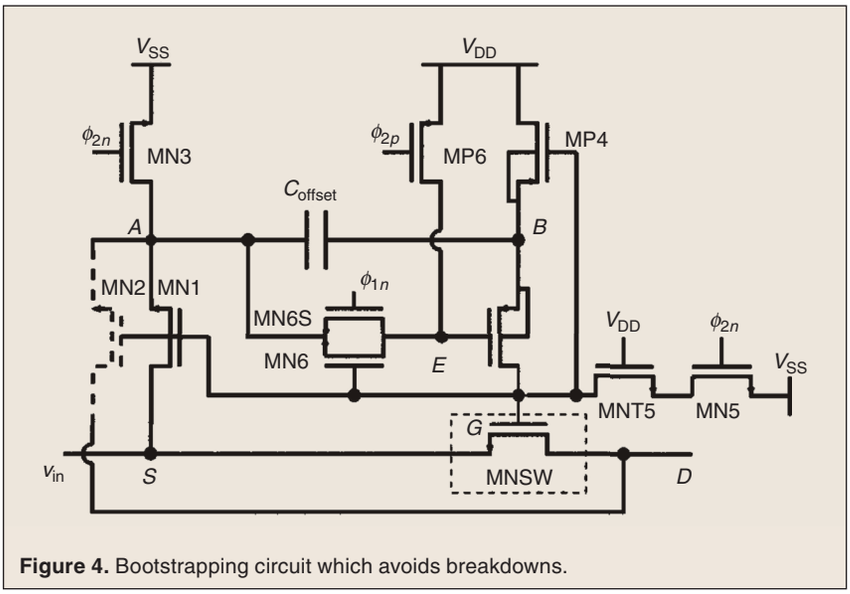

Figure 4. Bootstrapping circuit which avoids breakdowns.

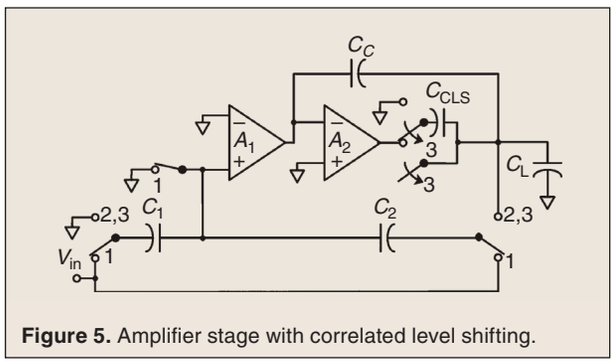

Figure 5. Amplifier stage with correlated level shifting.

next. The signal dependence of both Q_{ch} and R_{on} can be reduced by making the gate-channel voltage have a fixed value V_{dd} (Figure 2). Another problem may be that the clock voltage may be too low for turning on the switch. This may occur if the circuit is powered by a battery, or harvested energy. The clock voltage swing may be doubled by the scheme proposed by Y. Nakagome et al. and shown in Figure 3 [6]. Note that both the above arrangements may lead to overload and breakdowns, and have to be carefully examined. More complex switch driver circuits which avoid breakdown problems have also been found; a popular one is shown in Figure 4 [7].

There are also alternative strategies that completely eliminate the floating switch. These include the switched operational amplifier (opamp) circuit [8], which replaces the switch with a short circuit, and disables the driving amplifier during the discharging clock phase, and the reset opamp circuit [9] which sets it in a unity-gain configuration. Yet another method [10] replaces the floating switches with resistors.

Amplifiers have finite gain and bandwidth issues, and dc offset as well as 1/f and thermal noise and nonlinearity problems. Several of these nonideal effects can be mitigated by correlated double sampling [11] and correlated level shifting [12]. The former can cancel the dc offset, and high-pass the filter noise; the latter can reduce the output swing of the opamp, and thus also reduce distortion and finite gain effects. An example of a stage with correlated level shifting is illustrated in Figure 5.

In conclusion, switched-capacitor circuits are a good option for the implementation of accurate analog signal processing at low or medium frequencies. At high frequencies, continuous-time circuits may be preferable.

References

[1] J. C. Maxwell, *A Treatise on Electricity and Magnetism*, vol. 2. Oxford: Clarendon Press, 1873.

[2] D.L. Fried, "Analog sample-data filters," *IEEE J. Solid-State Circuits (JSSC)*, vol. 7, no. 4, pp. 302–304, Aug. 1972. doi: 10.1109/JSSC.1972.1050305.

[3] R. Gregorian, K.W. Martin, and G.C. Temes, "Switched-capacitor circuit design," *Proc. IEEE*, vol. 71, pp. 941–966, Aug. 1983. doi: 10.1109/PROC.1983.12700.

[4] G.C. Temes, "Simple formula for estimation of minimum clock feedthrough error voltage," *Electron. Lett.*, vol. 22, pp. 1069–1070, Sept. 1986. doi: 10.1049/el:19860733.

[5] T. C. Carusone, D. Johns, and K.W. Martin, *Analog Integrated Circuit Design*, 2nd ed. Hoboken, NJ: Wiley, 2012.

[6] Y. Nakagome et al., "Circuit techniques for 1.5-3.6-V battery-operated 64-Mb DRAM," *IEEE J. Solid-State Circuits*, vol. 26, pp. 1003-1010, July 1991.

[7] M. Dessouky and A. Kaiser, "Very low-voltage delta-sigma modulator with 88 dB dynamic range using local switch bootstrapping," *IEEE J. Solid-State Circuits*, vol. 36, pp. 349–355, Mar. 2001. doi: 10.1109/4.910473.

[8] M. Steyaert, J. Crois and S. Gogaert, "Switched-Opamp, a technique for realising full CMOS switched-capacitor filters at very low voltages," in *Proc. European Solid-State Circuits Conf.*, 1993.

[9] M. Keskin, U. Moon and G.C. Temes, "A 1-V 10-MHz clock-rate 13-Bit CMOS delta-sigma modulator using unity-gain-reset opamps," *IEEE J. Solid-State Circuits*, vol. 37, pp. 817-824, July 2002. doi: 10.1109/JSSC.2002.1015678.

[10] G. Ahn et al., "A 0.6 V 82 dB delta-sigma audio ADC using switched-RC integrators," *IEEE J. Solid-State Circuits*, vol. 40, pp. 2398–2407, Dec. 2005.

[11] H. Yoshizawa and G.C. Temes, "Switched-capacitor track-and-hold amplifiers with low sensitivity to opamp imperfections," *IEEE Trans. Circuits Syst.-I*, vol. 54, pp.193–199, Jan. 2007. doi: 10.1109/TCSI.2006.887454.

[12] B.R. Gregoire and U. Moon, "An over-60 dB true rail-to-rail performance using correlated level shifting and an opamp with 30 dB loop gain," in *Proc. IEEE Int. Symp. Solid-State Circuits*, 2008, pp. 540-541.